What is claimed is:

1. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure, wherein the first and second test procedures are adapted to test at least some different IC parameters, wherein the first tester is coupled to the second tester; and

a single handler coupled to the first and second testers.

2. The apparatus according to Claim 1, wherein the first tester is adapted to calibrate the second tester.

3. The apparatus according to Claim 2, wherein the second tester is adapted to submit a request for calibration to the first tester.

4. The apparatus according to Claim 2, wherein the first tester is adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount.

5. The apparatus according to Claim 1, wherein the first test procedure comprises at least one of static and dynamic current and voltage tests, dynamic functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing.

6. The apparatus according to Claim 1, wherein data is transmittable from the first tester to the second tester and/or from the second tester to the first tester

7. The apparatus according to Claim 1, further comprising a multiplexer coupled to the first and second testers, wherein the multiplexer is adapted to multiplex the first and second test procedures on the first and second IC's.

8. The apparatus according to Claim 7, wherein the first and second IC's are in die form integral to a single wafer, wherein the apparatus further comprises a wafer probe simultaneously coupleable to the first and second IC's.

9. The apparatus according to Claim 1, wherein the first and second testers comprise low cost testers.

10. The apparatus according to Claim 1, wherein the first and second testers comprise high cost testers.

11. The apparatus according to Claim 1, wherein first IC's that fail the first test procedures are moved to the second tester for testing with the second test procedure.

12. The apparatus according to Claim 1, further comprising:

control circuitry coupled to the first tester and second tester; and

storage means coupled to the control circuitry, first tester and second tester.

13. The apparatus according to Claim 12, wherein first and second IC test procedure result information is storable in the storage means with respect to first and second IC position.

14. The apparatus according to Claim 12, wherein the first and second IC's store identification information, wherein first and second IC test procedure result information is storable in the storage means with respect to the first and second IC identification information.

15. The apparatus according to Claim 1, wherein the apparatus is adapted to test the at least one first IC with the first tester first test procedure simultaneously while the at least one second IC is tested with the second tester second test procedure.

16. The apparatus according to Claim 1, wherein the first tester is indirectly coupled to the second tester by a host computer or host network.

17. The apparatus according to Claim 1, wherein the first tester is integral to the second tester.

18. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure;

a single handler coupled to the first and second testers; wherein the first and second test procedures are adapted to test at least some different IC parameters;

a first environmental chamber coupled to the first tester; and

a second environmental chamber coupled to the second tester, wherein the first and second test procedures comprise subjecting the first and second IC's to different environmental tests.

19. An apparatus for testing at least one first integrated circuit (IC) and at least one second IC, comprising:

a first tester adapted to test the at least one first IC with a first test procedure;

a second tester adapted to test the at least one first IC with a second test procedure simultaneously while the first tester tests the at least one second IC with the first test procedure; and

a single handler coupled to the first and second testers, wherein the first and second test procedures are adapted to test at least some different IC parameters, and wherein the first tester is integral to the handler.

20. The apparatus according to Claim 19, wherein the second tester is integral to the handler.

21. A method of testing at least one first integrated circuit (IC) and at least one second IC in an apparatus comprising a first tester and a second tester coupled to a single handler, the method comprising:

coupling the first tester to the second tester;

testing the first IC with a first test procedure using the first tester; and

testing the second IC with the first test procedure simultaneously while testing the first IC's with a second test procedure using the second tester, wherein testing IC's with the first test procedure comprises testing at least some different IC parameters than testing IC's with the second test procedure.

22. The method according to Claim 21, further comprising calibrating the second tester with the first tester and/or calibrating the first tester with the second tester.

23. The method according to Claim 22, wherein the calibrating is in response to a request for calibration from the first or second tester.

24. The method according to Claim 22, wherein the first tester is adapted to calibrate the second tester at predetermined time intervals or when ambient temperature has changed by a predetermined amount.

25. The method according to Claim 21, further comprising transmitting data from the first tester to the second tester and/or transmitting data from the second tester to the first tester.

26. The method according to Claim 21, wherein the first test procedure comprises at least one of static and dynamic current and voltage tests, dynamic functional AC/DC tests, DC offset tests, AC timing relation tests, internal AC parametric tests, power supply current tests, leakage current tests, gain tests, and/or low speed digital pattern tests; and wherein the second test procedure comprises at least one of external AC parametric tests, signal-to-noise ratio tests, DSP-based AC tests, distortion tests, thermal soaks, RF tests, and/or high speed digital pattern tests with precision timing.

27. The method according to Claim 21, further comprising multiplexing the first and second test procedures on the first and second IC's.

28. The method according to Claim 27, wherein the first and second IC's are in die form integral to a single wafer, wherein the method further comprises coupling a wafer probe simultaneously coupleable to the first and second IC's to perform the first and second test procedures.

29. The method according to Claim 21, further comprising:

subjecting the first IC's to a first environmental test while performing the second test procedure; and

subjecting the second IC's to a second environmental test while performing the first test procedure, wherein the first environmental test is different from the second environmental test.

30. The method according to Claim 21, further comprising moving first IC's that fail the first test procedures to the second tester for testing with the second test procedure.

31. The method according to Claim 21, further comprising storing the first and second IC test procedure result information with respect to first and second IC position.

32. The method according to Claim 21, further comprising storing the first and second IC test procedure result information with respect to the first and second IC identification information.

33. The method according to Claim 21, further comprising simultaneously testing the second IC with the second test procedure while testing the first IC with the first test procedure.